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09/704,329	11/02/2000	David I.J. Glen	ATI-000153BT	4939

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EXAMINER	
JACKSON, JENISE E	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/704,329	GLEN, DAVID I.J.	
	Examiner	Art Unit	
	Jenise E Jackson	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 13-15, 17-19, 21-23* is/are rejected.

7)☒ Claim(s) *16,20 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Schwed(5592556).

3. As per claim 1, Schwed discloses a digital interface device for facilitating key encryption of a digital signal which is communicated from a computer system to an associated peripheral device(see col. 1, lines 57-67, col. 2, lines 5-25), where the associated peripheral device decrypts the communicated digital signal for use(see col. 2, lines 5-25), the interface device includes a digital output formatting circuitry associated with the output;(see col. 4, lines 51-67) a non-volatile RAM for containing a BIOS for controlling digital output formatting having a specific write-protectable area allocated for storing an encryption key flag at a flag address and encryption key data(see col. 7, lines 9-40, col. 9, lines 22-50); and the specific write-protectable area being rendered read-only when a predetermined flag value is stored at the flag address whereby encryption key data many be stored in the specific area of the non-volatile RAM in connection with storing the predetermined flag value at the flag address such that stored encryption data cannot be altered by a subsequent write operation to the non-volatile RAM(see col. 7, lines 9-40, col. 8, lines 42-60).

4. As per claim 2, Schwed discloses a first predetermined flag value at the flag address in association with the key encryption data in the specific write-protectable area which first flag value indicates encryption enablement(see col. 9, lines 22-50).

5. As per claim 3, Schwed discloses to receive either a first predetermined flag value at the flag address in association with the key encryption data in the specific write-protectable area which first flag value indicates encryption enablement or a second predetermined flag value at the flag address which second flag value indicates encryption disablement in which case the digital interface device is permanently disabled for using the key encryption(see col. 7, lines 9-40, col. 9, lines 22-50).

6. As per claim 4, Schwed discloses configured to receive the predetermined value any value other than a specific value which specific value enable writing into the write-protectable area(see col. 16, lines 59-67).

7. As per claim 5, Schwed discloses wherein the key flag is a combination of one or more values stored at the one or more flag addresses within the write protectable area(see col. 17, lines 10-27).

8. As per claim 6, Schwed discloses wherein the associated peripheral device is a digital display and the digital out is an output port for a digital video signal(see col. 5, lines 1-43).

9. As per claim 7, Schwed discloses a digital video interface card(see col. 2, lines 43-62).

10. As per claim 8, Schwed discloses wherein the specific write-protectable area is at least 512K bytes and located at an address range higher than an address range reserved for a BIOS(see col. 14, lines 9-39).

11. As per claim 9, Schwed discloses providing a digital interface device having a digital output, digital output formatting circuitry associated with the output, and a non-volatile RAM for containing a BIOS for controlling digital output formatting(see col. 7, lines 9-40, col. 8, lines 42-60); allocating a specific addressable area on the non-volatile RAM for storing an encryption key flag and encryption key data; and rendering the specific area read-only when a predetermined key flag value is written in the specific addressable area at a key flag address(see col. 7, lines 9-40, col. 9, lines 22-50).

12. As per claim 10, Schwed discloses writing a first predetermined flag value at the key flag address along with key encryption data in the specific area to enable key encryption(see col. 9, lines 22-50).

13. As per claim 11, Schwed discloses writing a first predetermined flag value at the key flag address along with key encryption data in the specific area to enable key encryption; or writing a second predetermined flag value at the key flag address to permanently disable key encryption using the specific area(see col. 2, lines 44-62, col. 3, lines 1-19).

14. As per claim 12, Schwed discloses storing a specific value in the key flag address at the time the specific addressable area is allocated wherein the predetermined key value is any value other than the specific value(see col. 9, lines 22-50).

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 13-15, 17-19, 21-23, rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi(6,845,450).

17. As per claim 13, Kobayahsi et al. discloses a digital video interface device for facilitating key encryption(see col. 4, lines 24-32) of a digital signal which is communicated from a computer system to an associated peripheral device(i.e. graphics controller)(see col. 1, lines 57-67, col. 2, lines 5-25), where the associated peripheral device decrypts the communicated digital signal for use(see col. 2, lines 5-25), the interface device includes a digital output formatting circuitry associated with the output;(see col. 4, lines 51-67) a non-volatile RAM for containing a BIOS for controlling digital output formatting having a specific write-protectable area allocated for storing an encryption key flag at a flag address and encryption key data(see col. 7, lines 9-40, col. 9, lines 22-50); and the specific write-protectable area being rendered read-only when a predetermined flag value is stored at the flag address whereby encryption key data many be stored in the specific area of the non-volatile RAM in connection with storing the predetermined flag value at the flag address such that stored encryption data cannot be altered by a subsequent write operation to the non-volatile RAM(see col. 7, lines 9-40, col. 8, lines 42-60).

18. As per claim 14, Kobayahsi discloses a first predetermined flag value at the flag address in association with the key encryption data in the specific write-protectable area which first flag value indicates encryption enablement(see col. 4, lines 14-32).

19. As per claim 15, Kobayashi discloses to receive either a first predetermined flag value at the flag address in association with the key encryption data in the specific write-protectable area

which first flag value indicates encryption enablement (see col. 4, lines 14-32, col. 5, lines 15-22).

20. As per claim 17, Kobayashi discloses wherein the key flag is a combination of one or more values stored at the one or more flag addresses within the write protectable area(see col. 4, lines 14-32).

21. As per claim 18, Kobayashi discloses wherein the associated peripheral device is a digital display and the digital out is an output port for a digital video signal(see col. 2, lines 19-26, col. 6, lines 28-43).

22. As per claim 19, Kobayashi discloses a digital video interface card(see col. 4, lines 1-23).

23. As per claim 21, Kobayashi discloses providing a digital interface device having a digital output, digital output formatting circuitry associated with the output, and a non-volatile RAM for containing a BIOS for controlling digital output formatting(see col. 5, lines 13-22); allocating a specific addressable area on the non-volatile RAM for storing an encryption key flag and encryption key data; and rendering the specific area read-only when a predetermined key flag value is written in the specific addressable area at a key flag address(see col. 4, lines 14-32, col. 5, lines 15-22).

24. As per claim 22, Kobayashi discloses writing a first predetermined flag value at the key flag address along with key encryption data in the specific area to enable key encryption(see col. 5, lines 13-33).

25. As per claim 23, Kobayashi discloses writing a first predetermined flag value at the key flag address along with key encryption data in the specific area to enable key encryption(see col. 6, lines 54-67);

26. As per claim 24, Kobayashi discloses storing a specific value in the key flag address at the time the specific addressable area is allocated wherein the predetermined key value is any value other than the specific value(see col. 9, lines 22-50).

27. Claims objected to as being rejected on base claims are, 16, and 24, in the prior art of copy protection and encrypted code control signal, fails to disclose or suggest, configured to receive as the predetermined value any value other than a specific value which specific value enables writing into the write-protectable area. In prior art that value that is received is the value that is written into the protected area. Claim 20 is also objected to as being rejected on base claims for the specific write protectable area is at least 512 bytes and located at an address range higher than an address range reserved for a BIOS.

Response to Amendment

28. The Applicant states that Schwed does not disclose a write-protect enablement. The Examiner disagrees with the Applicant. Schwed discloses write protect enablement, because the transmission of Schwed is encrypted in order to protect against eavesdroppers(see col. 9, lines 22-25).

29. The Applicant states that Schwed does not disclose allocating a specific addressable area for an encryption key flag and making that area read only when the flag is set. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jenise E Jackson whose telephone number is (571) 272-3791. The examiner can normally be reached on M-Th (6:00 a.m. - 3:30 p.m.) alternate Friday's.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jenise Jackson

February 6, 2005

Gilberto Barron Jr.

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